draft proposed **X3T10/1071D**
American National Standard

American National Standard for Information Systems - SCSI-3 Fast-20

Abstract

This standard defines mechanical, electrical, and timing requirements for the SCSI-3 Fast-20. This standard is intended to be used in conjunction with the SCSI-3 Parallel Interface Standard. The resulting interface facilitates the interconnection of computers and intelligent peripherals and thus provides a common interface specification for both systems integrators and suppliers of intelligent peripherals.

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719-574-0424

Document Distribution

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The developers of this standard have requested that holder's of patents that may be required for the implementation of the standard, disclose such patents to the publisher. However neither the developers nor the publisher have undertaken a patent search in order to identify which if any patents may apply to this standard.

As of the date of publication of this standard and following calls for the identification of patents that may be required for the implementation of this standard, no such claims have been made. No further patent search is conducted by the developer or publisher in respect to any standard it processes. No representation is made or implied that licenses are not required to avoid infringement in the use of this standard.

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Foreword

The SCSI-3 Fast-20 Parallel Interface (Fast-20) is designed to be used in conjunction with the SCSI-3 Parallel Interface (SPI) to provide efficient peer-to-peer I/O bus devices with up to 8, 16, or 32 devices depending on the data path widths implemented, including one or more hosts. Fast-20 defines the specific mechanical, electrical, and timing parameters to support transfer rates of 20, 40, or 80 megabytes per second corresponding to the data path width implemented.

When implementing Fast-20, the requirements of SPI apply except where superceded by this standard.

With any technical document there may arise questions of interpretation as new products are implemented. The X3 Committee has established procedures to issue technical opinions concerning the standards developed by the X3 organization. These procedures may result in SCSI Technical Information Bulletins being published by X3.

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Introduction

The SCSI-3 Fast-20 (Fast-20) standard is divided into eight major clauses:

Clause 1 is the scope.

Clause 2 enumerates the normative references that apply to this standard.

Clause 3 describes the definitions, symbols, abbreviations, and conventions used in this standard.

Clause 4 describes the overview (i.e., model of Fast-20).

Clause 5 describes the cable characteristics.

Clause 6 describes the electrical characteristics.

Clause 7 describes the bus timing.

Clause 10 describes the services provided.

Annexes A and B form an integral part of this Standard.

Annex C provides information regarding transmission lines and is not an integral part of this standard.

1 Scope

This standard defines the mechanical, electrical, and timing requirements of the SCSI-3 Fast-20 Transfer Protocol to allow conforming devices to inter-operate at the data transport level. Fast-20 only defines those requirements to support the Fast-20 data transfer rate using synchronous data transfers. Other requirements (e.g., connectors, asynchronous transfer timing, etc.) are defined in the SCSI-3 Parallel Interface (SPI). The mechanical, electrical, and timing requirements defined herein take precedence over those defined in SPI.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this International Standard. At the time of publication, the editions indicated were valid. The Standards are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

EIA/TIA RS-485-1985, Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multipoint Systems [1]

ANSI X3.253-1995, *Information Systems - SCSI-3 Parallel Interface*

> Note 1 - An implementation that uses differential transceivers is intended for use in conjunction with EIA/TIA RS-485.

ANSI X3T10/856D, *SCSI-3 Interlocked Protocol Standard*

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purposes of this Standard, the following definitions apply.

3.1.1 byte: An 8-bit construct.

3.1.2 contact: The electrically-conductive portion of a connector associated with a single conductor in a cable.

3.1.3 DATA BUS: A 8-bit DATA BUS, a 16-bit DATA BUS, or 32-bit DATA BUS

3.1.4 differential: A signalling alternative that employs differential drivers and receivers to improve signal-to-noise ratios and increase maximum cable lengths (also see 3.1.13 single-ended).

3.1.5 fast transfer: A fast synchronous data transfer.

3.1.6 mandatory: The referenced item is required to claim conformance with this standard.

3.1.7 megatransfers per second: The repetitive rate at which a million words of data are transferred across the bus. This is equivalent to megabytes per second on an 8-bit DATA BUS.

3.1.8 optional: The referenced item is not required to claim conformance with this standard, but if the item is implemented it shall conform to the definitions within this standard.

3.1.9 reserved: The term used for bits, fields, signals, and code values that are set aside for use in future standards.

3.1.10 signal assertion: The act of driving a signal to the true state.

3.1.11 signal negation: The act of performing a signal release or of driving a signal to the false state.

3.1.12 signal release: The act of allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition).

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1. Available from the Electronic Industries Association, 2001 Eye Street NW, Washington, D.C. 20006.

3.1.13 single-ended: A signalling alternative that employs single-ended drivers and receivers to increase circuit density (also see 3.1.4 differential).

3.1.14 slow transfer: A slow synchronous data transfer with negotiated transfer periods of at least 200 ns.

3.1.15 source (a signal): The act of either signal assertion, signal negation, or signal release.

3.1.16 transceiver: A device that implements both the bus receiver and transmitter functions.

3.1.17 word: In this standard, this term indicates a 1-byte, 2-byte, or 4-byte construct.

3.2 Symbols and abbreviations

AWG American Wire Gauge

EMC Electro-magnetic compatibility

ESD Electro-static discharge

SCSI Either SCSI-2 or SCSI-3.

3.3 Conventions

Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the glossary or in the text where they first appear. Names of signals and phases are in all upper-case. Lower-case is used for words having the normal English meaning.

Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field.

Numbers that are not immediately followed by lower-case "b" or "h" are decimal values.

Numbers immediately followed by lower-case "b" (xxb) are binary values.

Numbers immediately followed by lower-case "h" (xxh) are hexadecimal values.

4 General

The SCSI-3 Fast-20 Standard defines the cables, signal, and transceiver characteristics necessary to operate at 20 mega-transfers per second. The services necessary to communicate with an upper layer protocol are defined in the SCSI-3 Parallel Interface standard.

This standard defines an extension to the SCSI-3 Parallel Interface to provide higher data transfer rates. Only the specifications of the interface related to these higher data rates are contained in this standard.

5 Connecting devices

5.1 Connecting devices with single-ended transceivers

The maximum cumulative signal path length between terminators shall be 3.0 meters when using up to 4 maximum capacitance (25 pF) devices. The maximum cumulative signal path length between terminators, shall be 1.5 meters when using from five to eight maximum capacitance devices. Extending the device count beyond eight requires specification control beyond the minimum specified in this document. It is recommended that the devices be uniformly spaced between terminators with the end devices located as close as possible to the terminators.

For environments where all elements of the bus (cables, device interfaces, environmental noise and other parameters) are controlled to be better than minimally required, it may be possible to extend the path length and device count (see note 3 in 6.1.4).

The signal path shall be a controlled impedance environment with the following characteristic impedance:

a) 90 ohms $\pm$ 6 ohms for the REQ and ACK signals;
b) 90 ohms $\pm$ 10 ohms for all other signals.

The stub length shall not exceed 0,1 meter. The stub length is measured from the transceiver to the connection to the mainline SCSI bus. The spacing of devices on the mainline SCSI bus should be at least three times the stub length to avoid stub clustering (See Annex C).

The magnitude of the ground offset voltage between logic grounds on any two device connectors shall be less than 50 mV.

5.2 Connecting devices with differential transceivers

Twisted-pair cable (either twisted-flat or discrete wire twisted pairs) should be used with differential transceivers.

The maximum cumulative cable length shall be 25 meters.

The stub length shall not exceed 0,2 meter. The stub length is measured from the transceiver to the connection to the mainline SCSI bus. The spacing of devices on the mainline SCSI bus should be at least three times the stub length to avoid stub clustering (See Annex C).

6 SCSI parallel interface electrical characteristics

The Fast-20 parallel interface allows one of two transceiver alternatives:

a) single-ended drivers and receivers, in which one conductor of the each signal pair is active and one is grounded;
b) differential drivers and receivers, in which both conductors of each signal pair are active.

The single-ended and differential alternatives are mutually exclusive.

6.1 Single-ended alternative

6.1.1 Single-ended termination

All SCSI bus signals are common among all devices connected to the bus. All signal lines shall be terminated at both ends with a terminator that is compatible with the type of transceivers used in the SCSI devices. The termination points define the ends of the bus. These termination points may be internal to an SCSI device.

All single-ended signals not defined as RESERVED, GROUND, or TERMPWR shall be terminated exactly once at each end of the bus. The termination of each signal shall meet these requirements:

a) the terminators shall be powered by the TERMPWR line;
b) each terminator shall source current to the signal line whenever its terminal voltage is below 2,5 V d.c. and this current shall not exceed 24 mA for any line voltage above 0,2 V d.c.even when all other signal lines are driven at 4,0 V d.c.;
c) the terminator shall not source current to the signal line whenever its terminal voltage is above 3,24 V d.c.;
d) the voltage on all released signal lines shall be at least 2,5 V d.c.;
e) these conditions shall be met with any legal configuration of targets and initiators as long as at least one device is supplying TERMPWR;
f) the terminator at each end of the SCSI bus (see clause 5.1) shall add a maximum of 25 pF capacitance to each signal.

Terminators employing a 220 ohm resistor to 5 Volts and a 330 ohm resistor to ground on each signal shall not be used.

6.1.2 Single-ended output characteristics

Single-ended signals shall use active-negation drivers. Active-negation drivers have three states: asserted, negated, and high-impedance. Each signal sourced by an SCSI device shall have the following d.c. output characteristics when measured at the SCSI device's connector:

a) V_{OL} (low-level output voltage) = 0,0 to 0,5 V d.c. at I_{OL} = 48 mA (signal asserted);
b) V_{OH} (high-level output voltage) = 2,5 to 3,7 V d.c. (signal negated);

c) The output characteristics (signal negated) shall be constrained to operate in the non-shaded areas of figure 1.

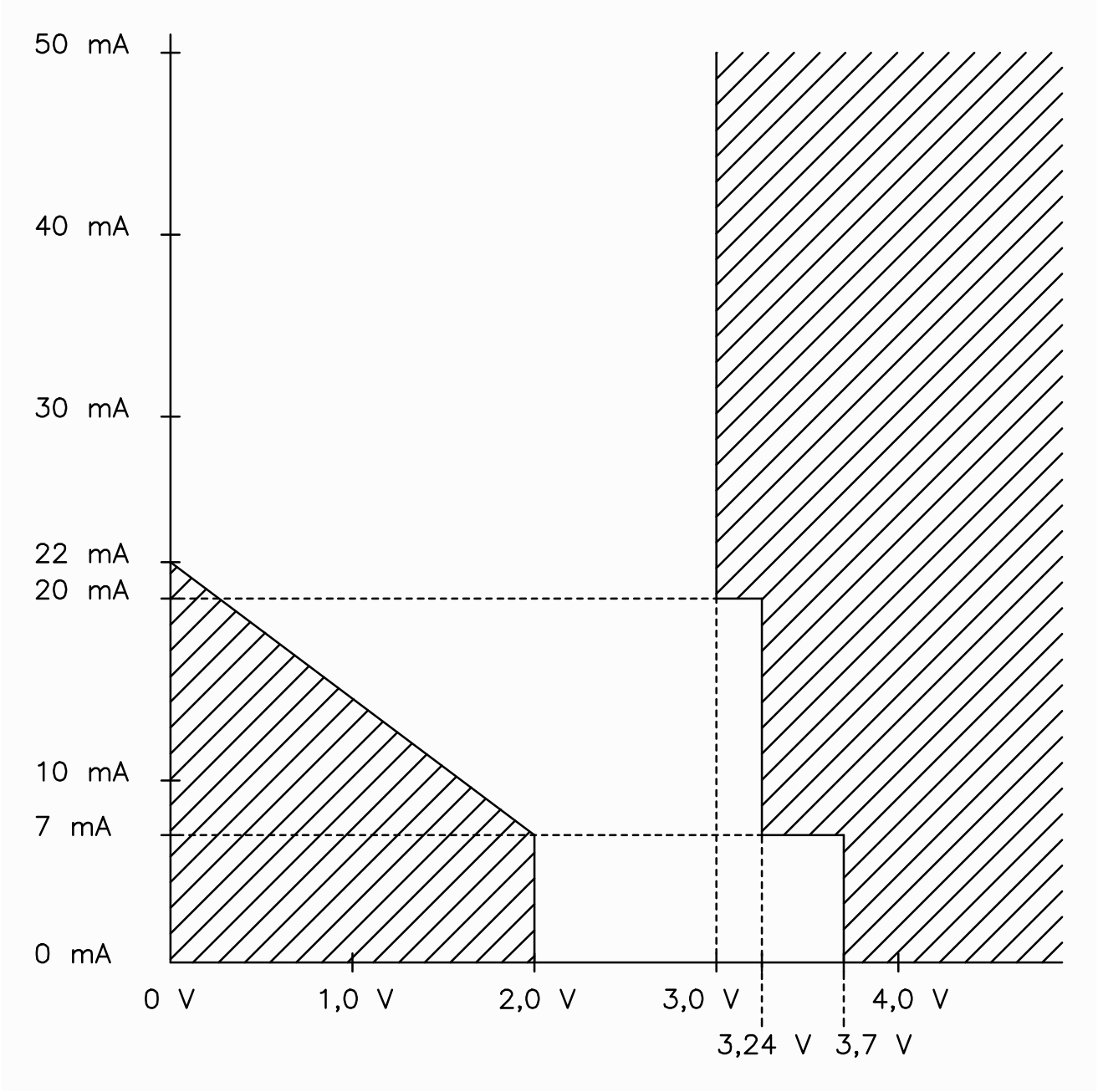


Figure 1 —Active negation current vs. voltage

Note: Figure 1 shows the allowed domains for the d.c. output characteristics of an active-negation driver when negated. It is not intended to show a.c. output characteristics, which may be different due to other requirements such as slew rate specifications. To measure the actual device d.c. output characteristics, it is necessary to vary the device load, so the test circuit shown in figure 2 is not applicable to this measurement

All single-ended drivers shall maintain the high-impedance state during power-on and power-off cycles.

SCSI devices should meet the following specifications for all signals when measured on the test circuit shown in figure 2 with a load capacitor (C_L) of 15 pF $\pm$ 5%:

a) t_{rise} (rise rate) = 520 mv per ns maximum (0,7 V d.c. to 2,3 V d.c.);

b) t_{fall} (fall rate) = 520 mv per ns maximum (2,3 V d.c. to 0,7 V d.c.).

All other output timing specifications shall be measured with the test circuit shown in figure 2 with a load capacitor (C_L) of 200 pF ± 5%.

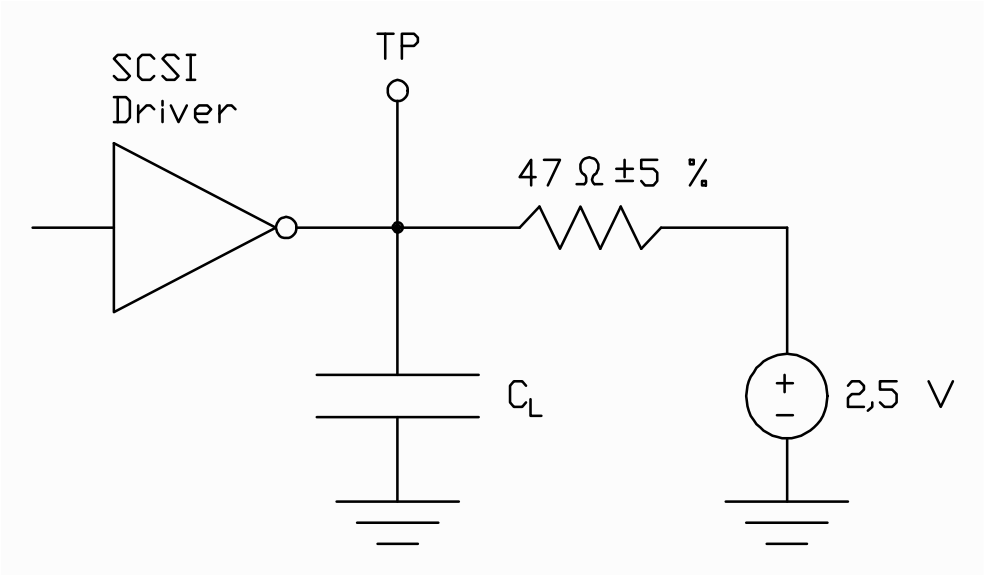


Figure 2 —Single-ended test circuit

6.1.3 Single-ended input characteristics

SCSI devices with power-on shall meet the requirements of Annex B and the following electrical characteristics on each signal (including both receivers and disabled drivers):

a) V_{IL} (Low-level input voltage) = 1,0 V d.c. maximum (signal true);
b) V_{IH} (High-level input voltage) = 1,9 V d.c. minimum (signal false);
c) I_{IL} (Low-level input current) = ± 20 uA at V_I = 0,5 V d.c.;
d) I_{IH} (High-level input current) = ± 20 uA at V_I = 2,7 V d.c.;
e) Minimum input hysteresis = 0,3 V d.c.

The transient leakage current that may occur (e.g. with some ESD protection circuits) at the time of physical insertion of an SCSI device is an exponentially decaying current that does not exceed the following specifications:

a) $I_{IH.HP}$ (hot-plug high-level input current peak value excluding the first 10 ns) = + 1.5 mA at V_I = 2,7 V d.c.;
b) T_{HP} (transient current duration to 10% of peak value) = 20 us maximum.

If the transfer period is greater than or equal to 100 ns then the REQ/REQQ and ACK/ACKQ glitch-filter as defined within SPI applies.

SCSI devices with power-off should meet the above I_{IL} and I_{IH} electrical characteristics on each signal, except at time of physical insertion, when $I_{IH.HP}$ and T_{HP} prevail.

Note 2 - Due to the tighter voltage thresholds for Fast-20, the power supply should have a maximum ± 5% tolerance of the nominal voltage.

6.1.4 Single-ended input and output characteristics

The single-ended signals shall have the following characteristics when measured at the SCSI device's connector:

a) I_L (Leakage current) = -20 uA to +20 uA at V_I = 0,0 to 3,7 V d.c. (high-impedance state);
b) Maximum signal capacitance = 25 pF, measured at the beginning of the stub (see annex B).

Note 3 - Devices with a careful board design using the latest semiconductor technology can lower the lumped capacitance to less than 16 pF. Devices without a switchable terminator can reduce this node capacitance even further. A decrease in lumped capacitance of the node and a uniform increase of the impedance along the SCSI bus towards 90 ohms improves the margin and may allow for a greater number of attached devices. Backplane designs give the implementor the possibility to increase the margins and connect a greater number of devices to the bus.

6.2 Differential alternative

6.2.1 Differential termination

All SCSI bus signals are common among all devices connected to the bus. All signal lines shall be terminated at both ends with a terminator that is compatible with the type of transceivers used in the SCSI devices. The termination points define the ends of the bus.

All differential signals consist of two lines denoted +SIGNAL and -SIGNAL. A signal is true when +SIGNAL is more positive than -SIGNAL, and a signal is false when -SIGNAL is more positive than +SIGNAL. All assigned differential signals described in the SCSI-3 Parallel Interface except TERMPWR, RESERVED, and GROUND shall be terminated at each end of the cable with a terminator network as shown in figure 3. Resistor tolerances in the terminator network shall be 5% or less. The differential characteristic impedance of differential terminators is 122 ohms.

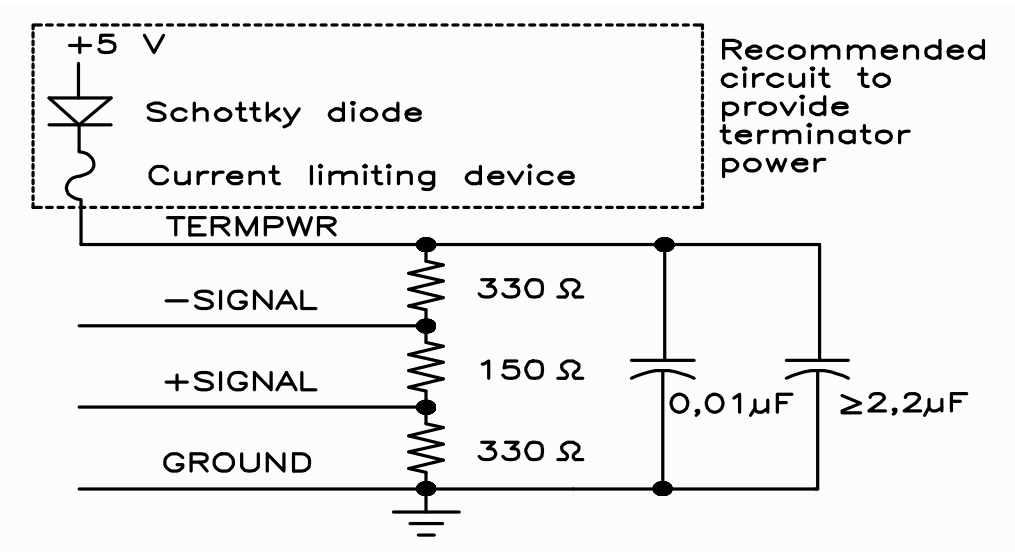


Figure 3 —Termination for differential devices

6.2.2 Differential output characteristics

The electrical characteristics of the drivers shall conform to EIA/TIA RS-485-1985 and all differential drivers shall maintain a high output impedance during power-on and power-off cycles.

6.2.3 Differential input characteristics

The input characteristics of each differential signal pair, when measured at the SCSI device's connector, shall

a) conform to EIA/TIA RS-485-1985;
b) exhibit at least 35 mV of hysteresis;
c) measure no more than 25 pF of capacitance.

6.2.4 Single-ended driver protection

The DIFFSENS signal is a single-ended signal that is used as an active high enable for the differential drivers. If a single-ended device or terminator is inadvertently connected, this signal is grounded, disabling the differential drivers to protect the single-ended drivers (see figure 4).

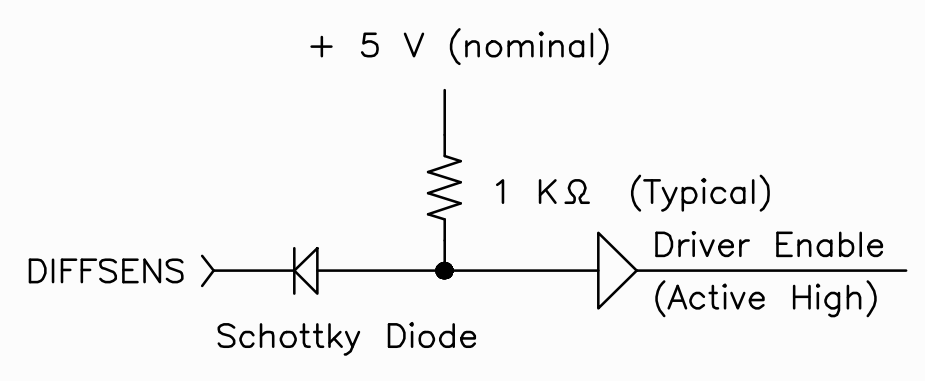


Figure 4 —Single-ended driver protection circuit

Table 1 —SCSI bus timing values

Timing description	fast-20	fast	slow	asynch
Arbitration Delay	2,4 us	2,4 us	2,4 us	2,4 us
Bus Clear Delay	800 ns	800 ns	800 ns	800 ns
Bus Free Delay	800 ns	800 ns	800 ns	800 ns
Bus Settle Delay	400 ns	400 ns	400 ns	400 ns
Cable Skew Delay (note 1)	3 ns	4 ns	4 ns	4 ns
Data Release Delay	400 ns	400 ns	400 ns	400 ns
Receive Assertion Period (note 6)	11 ns	22 ns	70 ns	n/a
Receive Hold Time (note 2 and note 6)	11,5 ns	25 ns	25 ns	n/a
Receive Negation Period (note 6)	11 ns	22 ns	70 ns	n/a
Receive Setup Time (note 2 and note 6)	6,5 ns	15 ns	15 ns	n/a
Reset Hold Time	25 us	25 us	25 us	25 us
Selection Abort Time	200 us	200 us	200 us	200 us
Selection Time-out Delay (note 3)	250 ms	250 ms	250 ms	250 ms
System Deskew Delay	15 ns	20 ns	45 ns	45 ns
Transfer Period during Synchronous Data Transfer Phases (note 5)	50 ns	100 ns	200 ns	n/a
Transmit Assertion Period (note 6)	15 ns	30 ns	80 ns	n/a
Transmit Hold Time (note 2 and note 6)	16,5 ns	33 ns	53 ns	n/a
Transmit Negation Period (note 6)	15 ns	30 ns	80 ns	n/a
Transmit Setup Time (note 2 and note 6)	11,5 ns	23 ns	23 ns	n/a

Notes -
1) This time does not apply at the SCSI device connectors.
2) See Annex A for examples of how to calculate setup and hold timing.
3) This is a recommended time. It is not mandatory.
4) The fast, slow, and asynch times are shown for reference only.
5) The transfer period is measured from an assertion edge of REQ/REQQ (ACK/ACKQ) signal to the next assertion edge of the signal.
6) See Annex B for Fast-20 timing specifications.

Annex A

(normative)

Setup and hold timing

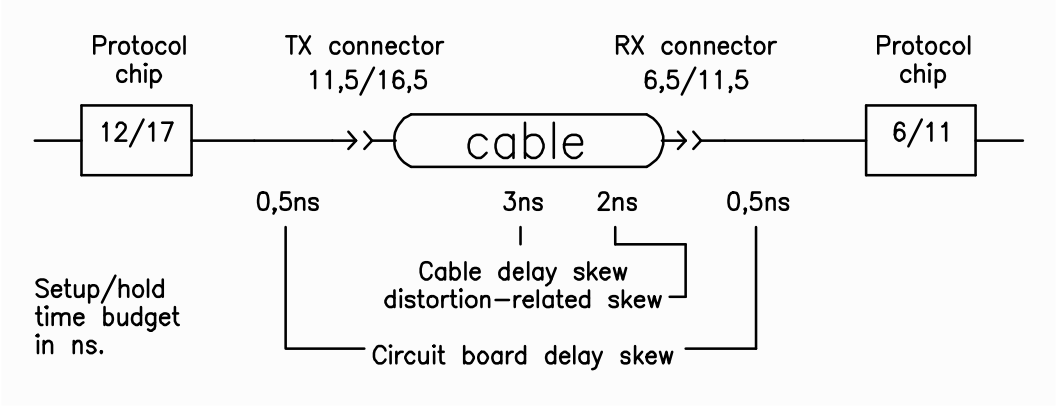


Figure A.1— Fast-20 setup and hold times for single-ended applications

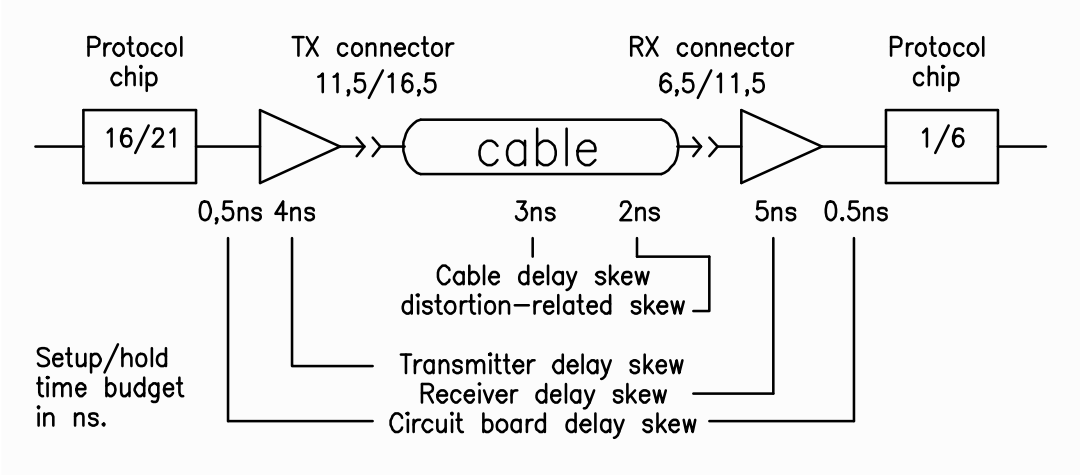


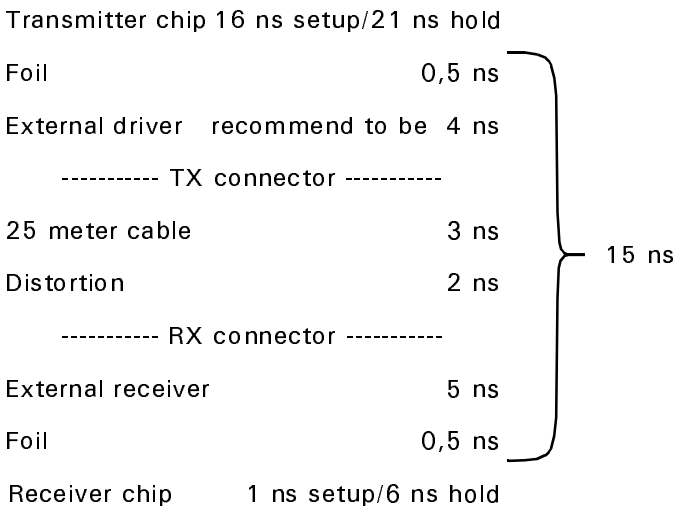
Figure A.2— Fast-20 setup and hold timing for differential applications

The receiver delay skew is the maximum difference in propagation delay time between any two receivers on the REQ, REQQ, ACK, ACKQ, DATA BUS, or parity signals of the same bus when external receivers are used.

The transmitter delay skew is the maximum difference in propagation delay time between any two transmitters on the REQ, REQQ, ACK, ACKQ, DATA BUS, or parity signals of the same bus when external transmitters are used.

The cable delay skew includes skew caused by non-uniform bus loading in mixed width applications, path length differences between different signals, and other factors affecting propagation time differences between the connectors between different signals.

In systems with external transceivers, the total skew budget is 15 ns.



At its connector, the transmitting SCSI device should:

a) drive data no less than 11,5 ns before asserting the REQx or ACKx signal;
b) keep that data valid for no less than 16,5 ns following the assertion of the REQx or ACKx signal.

The receiving device shall be able to latch the data at its connector when:

a) data is valid no more than 6,5 ns prior to the false-to-true transition of the REQx or ACKx signal;
b) data is valid no more than 11,5 ns following the false-to-true transition of REQx or ACKx signal.

When 4,5 ns is added to the transmit device timing for transmitter skew and skew due to foil delays, the transmitting SCSI chip setup and hold timings are 16 ns and 21 ns, respectively. Similarly, when 5,5 ns is subtracted from the skew budget of the receiving device, 1 ns and 6 ns are left for the receiving SCSI chip setup and hold, respectively.

In the case of fast-20 timing with no external transceivers over a 3 m signal path, the total skew budget is 6 ns, compared to 15 ns. The 9 ns difference is used to relax the timing at the SCSI protocol chips (4 ns for the transmitting chip, and 5 ns for the receiving chip).

Note 4: Component vendors may require that differential drivers and receivers be operated within restricted voltage and temperature differences to achieve the specified transmitter and receiver delay skew values.

Annex B

(normative)

Measurement of fast-20 timings on a single ended bus

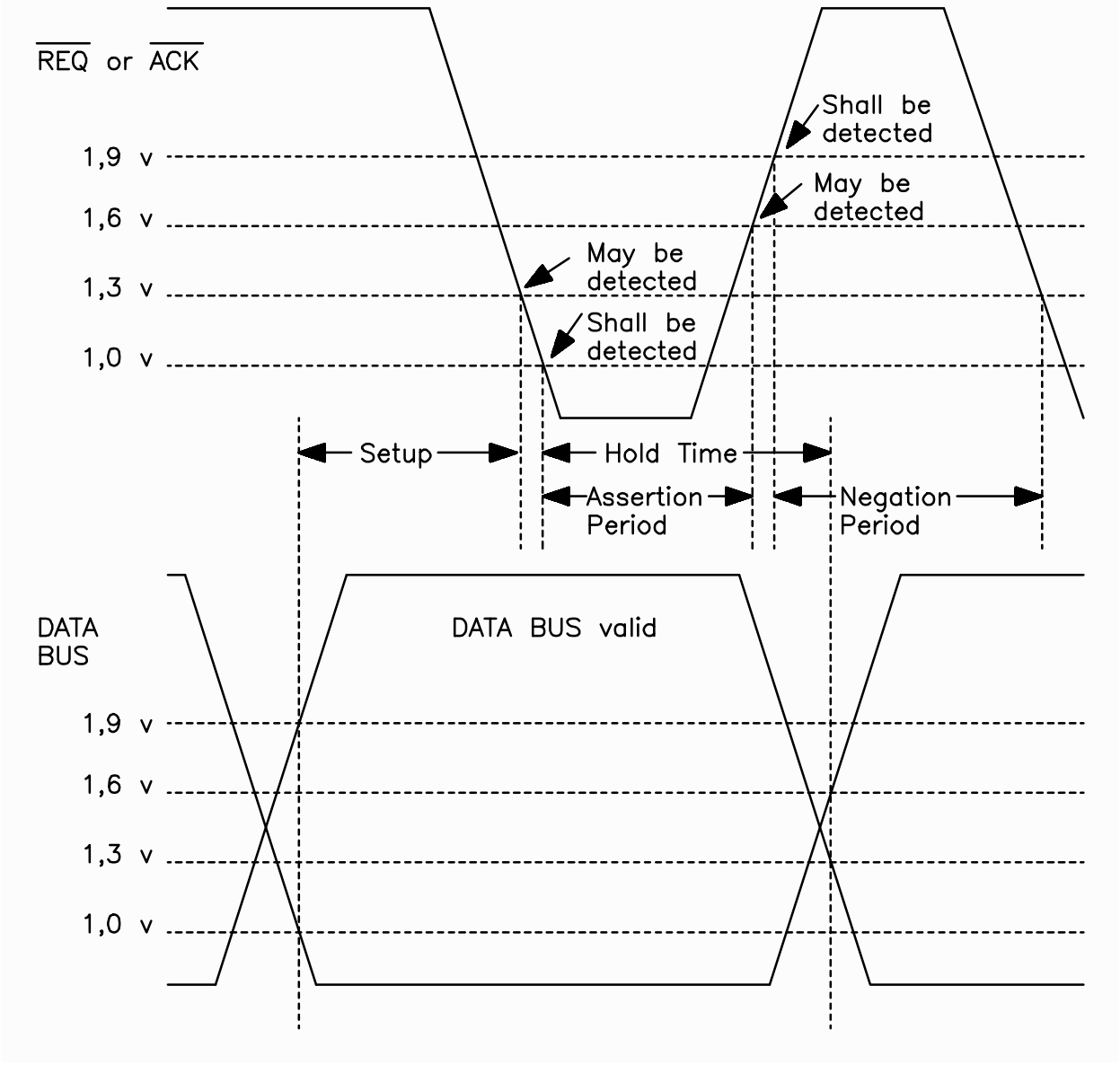


Figure B.1 — Fast-20 single-ended timing measurements

Annex C

(informative)

Transmission line considerations

The SCSI bus is a distributed parameter circuit whose electrical characteristics and responses are primarily defined by the distributed inductance and capacitance along the physical media. The media is defined here as the interconnecting cable(s) or conducting paths, connectors, terminators, and SCSI devices added along the bus. The following analysis derives a guideline for the amount of capacitance (and its spacing) that can be added to the Single-ended Fast-20 SCSI bus.

To a good approximation, the characteristic transmission line impedance seen into any cut point in the unloaded SCSI bus is defined by $Z = \sqrt{\frac{L}{C}}$, where L is the inductance per unit length and C is the capacitance per unit length. As capacitance is added to the bus, in the form of devices and their interconnection, the bus impedance is lowered and can be expressed by $Z' = \sqrt{\frac{L}{(C + C')}}$, where C' is the added capacitance per unit length. When capacitance is added to the bus by devices, an impedance mismatch occurs. When a signal wave arrives at this mismatch in impedance, an attenuation (or amplification) of the signal will occur. The magnitude of the attenuation will depend upon the ratio of the mismatched impedance or $A = \frac{Z'}{Z}$, where Z' is the load impedance and Z is the source impedance.

Substituting the equations for Z' and Z and reducing,

1) $$A = \frac{Z'}{Z} = \frac{\sqrt{\frac{L}{(C + C')}}}{\sqrt{\frac{L}{C}}} = \sqrt{\frac{1}{\left(1 + \frac{C'}{C}\right)}}$$

We now have a relationship for the attenuation of the signal voltage at an impedance mismatch due to load capacitance distributed on the SCSI bus. Next, a rule for the ratio of Z' to Z will be derived.

With fast transfer rates and electrically long[1] media, it becomes essential to achieve a valid input voltage level on the first signal transition from an output driver anywhere on the bus. This is called incident-wave switching. If incident-wave conditions are not achieved, reflected-wave switching must be used. Reflected-wave switching depends upon reflected energy occurring some time after the first transition arrives to achieve a valid logic voltage level.

In the Fast-20 SCSI environment, the valid low-level input voltage threshold has been raised and the high-level input voltage threshold has been lowered to allow incident-wave switching with some inevitable impedance mismatching and signal attenuation along the media.

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1. Electrically long is defined here as $\tau > \frac{t_{10-90\%}}{3}$, where τ is the one-way time delay across the bus and $t_{10-90\%}$ is the 10% to 90% transition time of the fastest driver output signal.

The signal voltage at an impedance mismatch is $V_{L1} = V_{L0} + V_{J1} + V_{R1}$, where V_{L0} is the initial voltage, V_{J1} is the input signal voltage, and V_{R1} is the reflected voltage. The voltage reflected back from the mismatch is $V_{R1} = \rho_L \times V_{J1}$ where, $\rho_L = \frac{Z' - Z}{Z' + Z}$ and is the coefficient of reflection commonly used in transmission line analysis. The voltage equation can now be written as $V_{L1} = V_{L0} + V_{J1} + (\rho_L \times V_{J1})$.

When an SCSI signal is asserted, the V_{L0} can be at a maximum of 3,7 V and go to 0 V (for a perfect driver) giving a V_{J1} of -3,7 V and the signal voltage must go below the minimum receiver input voltage threshold of 1 V. In equation form,

$$1 > (3,7) + (-3,7) + (\rho_L \times (-3,7))$$
$$\rho_L > \frac{1 - 3,7 + 3,7}{-3,7} = -0,27 \quad .$$

The negative value means that no more than 27% of the input signal voltage can be reflected back towards the source or the minimum assertion level will not be achieved by the incident wave[1].

Now, to relate this to Z'/Z and solving equation 1) for C'/C,

2)
$$\rho_L = \frac{Z' - Z}{Z' + Z} > -0,27$$
$$Z' - Z > -0,27 \times (Z' + Z)$$
$$Z' \times (1 + 0,27) > Z \times (1 - 0,27)$$
$$\frac{Z'}{Z} > (0,73/1,27) = 0,57$$

and

$$0,57 < \sqrt{\frac{1}{\left(1 + \frac{C'}{C}\right)}}$$
$$\frac{1}{0,57^2} - 1 > \frac{C'}{C}$$
$$\frac{C'}{C} < 2,08$$

We can now say that capacitance should not be added at more than twice the bus distributed capacitance for incident-wave switching. For example, a cabled bus with L = 295 nH/m (90 nH/ft) and C = 41 pF/m (12,5 pF/ft) and Z = 85 ohms, the guideline becomes to add no more than 85 pF/m (26 pF/ft) anywhere along the bus. This guideline can be met by 25 pF loads spaced 0,3 m (1 ft) from each other, 50 pF spaced 0,6 m (2 ft) apart, or 12,5 pF spaced 0,15 m (0,5 ft) apart. This relationship is shown graphically in figure

1. A similar analysis can be used for the negation case of 0 V to 2,8 V ([48 mA + 22 mA] x 40Ω) and an input voltage threshold of 1,9 V for a minimum reflection coefficient of -0,32. This leaves assertion as the most restrictive case.

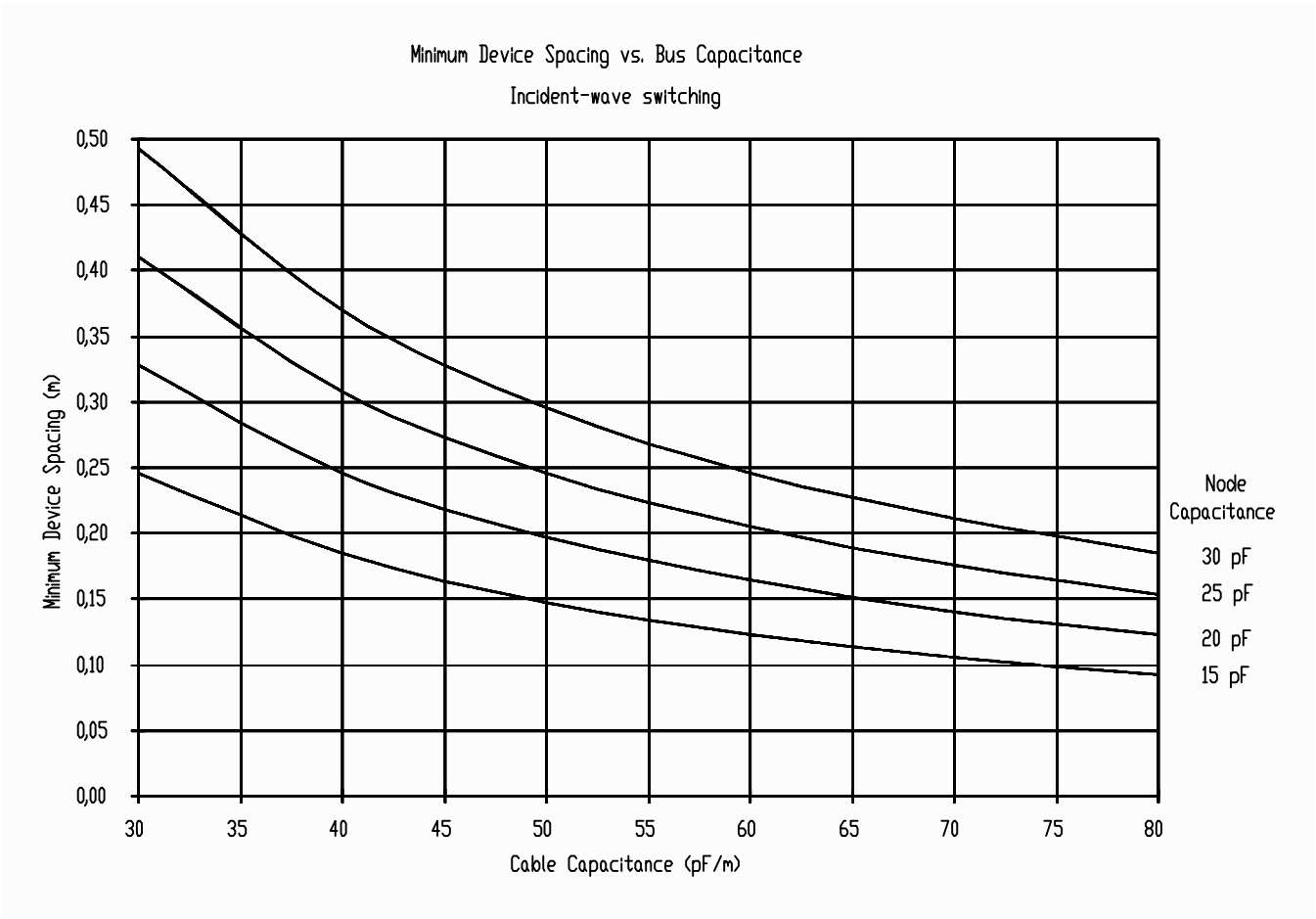

Figure C.1— Minimum device spacing versus bus and device capacitance